IN THE CLAIMS:

Claims 1-20. (**Cancelled**)

Claim 21. (**Previously Presented**) A semiconductor integrated circuit, comprising:

a pattern layer where a plurality of fundamental cells and a plurality of connector terminals are formed;

a first metal wiring layer, provided above the pattern layer, where no fixed power supply wiring extending to the fundamental cells is formed; and

a second metal layer, provided above the first metal wiring layer, where the fixed power supply wiring extending to the fundamental cells is formed; and

wherein the plurality of fundamental cells and the fixed power supplies are connected via the plurality of connector terminals.

Claim 22. (**Cancelled**)

Claim 23. (**Cancelled**)

Claim 24. (**New**) A fundamental cell according to claim 21, further comprising:

more than two types of the connector terminals, wherein:

the wiring directions of wirings connected to the connector terminals and wired between the fundamental cells are in different wiring direction from each other including first and second directions perpendicular to each other.

Claim 25. (**New**) A fundamental cell according to claim 21, wherein:

the connector terminals have the same wiring layers as the wirings to be wired between the fundamental cells.

Claim 26. (**New**) A fundamental cell according to claim 21, wherein:

the connector terminals have stacked VIAs including the same wiring layers as the wiring to be wired between the fundamental cells.

Claim 27. (**New**) A fundamental cell according to claim 21, wherein:

the wirings to be wired between the fundamental cells are wirings for interconnecting the fundamental cells, block cells having more than two of the fundamental cells to perform specific circuit operations, and macro cells having more than two of the block cells.

Claim 28. (**New**) A fundamental cell according to claim 21, wherein:

the wirings to be wired between the fundamental cells includes

power source lines or ground potential lines,

the connector terminals include

power source terminals or ground potential terminals to the fundamental cell.

Claim 29. (**New**) A semiconductor integrated circuit device according to claim 21, wherein a wiring direction and a wiring width of the fixed power supply wiring are appropriately selected for connecting.

Claim 30. (**New**) A semiconductor integrated circuit device according to claim 21, wherein a wiring width of the fixed power supply wiring exceeds the fundamental cell.

Claim 31. (**New**) A semiconductor integrated circuit device according to claim 21, wherein the fixed power supply wiring forms bypassing routes for bypassing around a wiring prohibited area.